CLAIMS

1. A refresh controller for use in a dynamic random access memory ("DRAM") having a full density mode and a reduced density mode, the refresh controller comprising:

an oscillator generating a first periodic clock signal;

a frequency division circuit coupled to receive the periodic clock signal, the frequency division circuit being operable to generate a second periodic clock signal having a frequency that is less than the frequency of the first periodic signal;

a first selector circuit coupled to receive the first periodic clock signal from the oscillator and the second periodic clock signal from the frequency division circuit, the first selector circuit being operable to apply the first periodic clock signal to an output terminal in the full density mode and to apply the second periodic clock signal to the output terminal in the reduced density mode;

a counter having a clock input terminal coupled to the output terminal of the first selector circuit, the counter having first and second stages the first of which increments at a faster rate than the second; and

a second selector circuit coupled the first and second stages of the counter, the second selector circuit being operable to couple the first stage of the counter to an output terminal in the full density mode and being operable to couple the second stage of the counter to the output terminal in the reduced density mode.

2. The refresh controller of claim 1 wherein the first selector circuit comprises:

a first pass gate coupled between an output of the oscillator and the clock input terminal of the counter;

a second pass gate coupled between an output of the frequency division circuit and the clock input terminal of the counter; and

a control circuit for enabling the first pass gate and disabling the second pass gate in the full density mode and for disabling the first pass gate and enabling the second pass gate in the reduced density mode.

3. The refresh controller of claim 1 wherein the second selector circuit comprises:

a first pass gate coupled between the first stage of the counter and the output terminal;

a second pass gate coupled between the second stage of the counter and the output terminal; and

a control circuit for enabling the first pass gate and disabling the second pass gate in the full density mode and for disabling the first pass gate and enabling the second pass gate in the reduced density mode.

4. The refresh controller of claim 1 wherein the second stage of the counter is two stages from the first stage of the counter so that the second stage is incremented at one-quarter the rate of the first stage.

5. The refresh controller of claim 1 wherein the frequency divider circuit comprises a toggle flip-flop.

6. The refresh controller of claim 1 wherein the reduced density mode comprises a half density mode.

7. A refresh controller for use in a dynamic random access memory ("DRAM") having a full density mode and a reduced density mode, the refresh controller comprising:

an oscillator generating a first periodic clock signal;

a frequency division circuit coupled to receive the periodic clock signal, the frequency division circuit being operable to generate a second periodic clock signal having a frequency that is less than the frequency of the first periodic signal; and

a selector circuit coupled to receive the first periodic clock signal from the oscillator and the second periodic clock signal from the frequency division circuit, the first selector circuit being operable to apply the first periodic clock signal to an output terminal in the full density mode and to apply the second periodic clock signal to the output terminal in the reduced density mode.

8. The refresh controller of claim 7 wherein the selector circuit comprises:

a first pass gate coupled between an output of the oscillator and the output terminal;

a second pass gate coupled between an output of the frequency division circuit and the output terminal; and

a control circuit for enabling the first pass gate and disabling the second pass gate in the full density mode and for disabling the first pass gate and enabling the second pass gate in the reduced density mode.

9. The refresh controller of claim 7 wherein the frequency divider circuit comprises a toggle flip-flop.

10. The refresh controller of claim 7 wherein the reduced density mode comprises a half density mode.

11. A refresh controller for use in a dynamic random access memory ("DRAM") having a full density mode and a reduced density mode, the refresh controller comprising:

an oscillator generating a periodic clock signal;

a counter having a clock input terminal coupled to receive the clock signal, the counter having first and second stages the first of which increments at a faster rate than the second; and

a selector circuit coupled the first and second stages of the counter, the selector circuit being operable to couple the first stage of the counter to an output terminal in the full density mode and being operable to couple the second stage of the counter to the output terminal in the reduced density mode.

12. The refresh controller of claim 11 wherein the selector circuit comprises:

a first pass gate coupled between the first stage of the counter and the output terminal;

a second pass gate coupled between the second stage of the counter and the output terminal; and

a control circuit for enabling the first pass gate and disabling the second pass gate in the full density mode and for disabling the first pass gate and enabling the second pass gate in the reduced density mode.

13. The refresh controller of claim 11 wherein the second stage of the counter is two stages from the first stage of the counter so that the second stage is incremented at one-quarter the rate of the first stage.

3 14. The refresh controller of claim 11 1 wherein the reduced density mode comprises a half density mode.

15. A refresh controller for use in a dynamic random access memory ("DRAM") having a full density mode and a reduced density mode, the refresh controller comprising:

a toggle circuit receiving an auto refresh command and being structured to generate an enable signal responsive to only a portion of a plurality of auto-refresh commands;

a gate having a first input coupled to the toggle circuit and a second input receiving each of the plurality of auto-refresh commands, the gate being structured to generate a refresh signal responsive to each auto-refresh command when the gate is enabled by the enable signal from the toggle circuit.

16. The refresh controller of claim 15 wherein the reduced density mode comprises a half density mode.

17. A circuit for remapping a specific row address bit to a specific column address bit, comprising:

a first latch coupled to receive the specific row address bit, the latch being operable to store the specific row address bit responsive to a row address strobe signal and to then output the stored row address bit;

a second latch coupled to receive a first set of column address bits and the specific column address bit, the latch being operable to store the first set of column address bits and the specific column address bit responsive to a column address strobe signal and to then output the stored column address bits, including the specific column address bit; and

a selector operable to select either the specific row address bit output from the first latch or the specific column address bit output from the second latch, the selected address bit being combined with the column address bits in the first set.

18. The remapping circuit of claim 17 wherein the selector comprises:

a first pass gate coupled between an output of the first latch and an address output terminal;

a second pass gate coupled between an output of the second latch and the address output terminal; and

a control circuit for enabling the first pass gate and disabling the second pass gate or disabling the first pass gate and enabling the second pass gate.

19. A dynamic random access memory ("DRAM") comprising:

an array of memory cells arranged in rows and columns;

a column address latch structured to store a column address responsive to a column address strobe signal;

a column decoder coupled to the column address latch to receive the stored column address and enable respective sense amplifiers corresponding thereto;

a row address latch structured to store a row address responsive to a row address strobe signal;

a first row decoder coupled to the row address latch to receive the stored row address and activate respective word lines corresponding thereto, the first row decoder being enable responsive to a first enable signal;

a second row decoder coupled to the row address latch to receive the stored row address and activate respective word lines corresponding thereto, the row lines activated by the first row decoder being interleaved with the row lines activated by the second row decoder, the second row decoder being enabled responsive to a second enable signal;

a mode controller coupled to the row decoders, the mode controller being operable in the full density mode to generate the first enable signal responsive to a first state of a least significant bit of the row address and to generate the second enable signal responsive to a second state of the least significant bit of the row address, the mode controller further being operable to generate the first and second enable signals in a reduced density mode regardless of the state of the least significant bit of the row address;

a data path coupled between the memory array and a data terminal; and

a refresh controller for refreshing at least some of the memory cells in the memory array responsive to a refresh trigger signal, the refresh controller comprising:

an oscillator generating a first periodic clock signal;

a frequency division circuit coupled to receive the periodic clock signal, the frequency division circuit being operable to generate a second periodic clock signal having a frequency that is less than the frequency of the first periodic signal;

a first selector circuit coupled to receive the first periodic clock signal from the oscillator and the second periodic clock signal from the frequency division circuit, the first selector circuit being operable to apply the first periodic clock signal to an output terminal in a full density mode and to apply the second periodic clock signal to the output terminal in a reduced density mode;

a counter having a clock input terminal coupled to the output terminal of the first selector circuit, the counter having first and second stages the first of which increments at a faster rate than the second; and

a second selector circuit coupled the first and second stages of the counter, the second selector circuit being operable to couple the first stage of the counter to an output terminal in the full density mode and being operable to couple the second stage of the counter to the output terminal in the reduced density mode, the refresh trigger signal being generated responsive to the counter stage coupled to the output terminal by the second selector circuit being incremented or decremented.

20. The dynamic random access memory of claim 19 wherein the first selector circuit comprises:

a first pass gate coupled between an output of the oscillator and the clock input terminal of the counter;

a second pass gate coupled between an output of the frequency division circuit and the clock input terminal of the counter; and

a control circuit for enabling the first pass gate and disabling the second pass gate in the full density mode and for disabling the first pass gate and enabling the second pass gate in the reduced density mode.

21. The dynamic random access memory of claim 19 wherein the second selector circuit comprises:

a first pass gate coupled between the first stage of the counter and the output terminal;

a second pass gate coupled between the second stage of the counter and the output terminal; and

a control circuit for enabling the first pass gate and disabling the second pass gate in the full density mode and for disabling the first pass gate and enabling the second pass gate in the reduced density mode.

22. The dynamic random access memory of claim 19 wherein the second stage of the counter is two stages from the first stage of the counter so that the second stage is incremented at one-quarter the rate of the first stage.

23. The dynamic random access memory of claim 19 wherein the frequency divider circuit comprises a toggle flip-flop.

24. A dynamic random access memory ("DRAM") comprising:

an array of memory cells arranged in rows and columns;

a column address latch structured to store a column address responsive to a column address strobe signal;

a column decoder coupled to the column address latch to receive the stored column address and enable respective sense amplifiers corresponding thereto;

a row address latch structured to store a row address responsive to a row address strobe signal;

a first row decoder coupled to the row address latch to receive the stored row address and activate respective word lines corresponding thereto, the first row decoder being enable responsive to a first enable signal;

a second row decoder coupled to the row address latch to receive the stored row address and activate respective word lines corresponding thereto, the row lines activated by the first row decoder being interleaved with the row lines activated by the second row decoder, the second row decoder being enabled responsive to a second enable signal;

a mode controller coupled to the row decoders, the mode controller being operable in a full density mode to generate the first enable signal responsive to a first state of a least significant bit of the row address and to generate the second enable signal responsive to a second state of the least significant bit of the row address, the mode controller further being operable to generate the first and second enable signals in a reduced density mode regardless of the state of the least significant bit of the row address;

a data path coupled between the memory array and a data terminal; and

a refresh controller for refreshing at least some of the memory cells in the memory array responsive to a refresh trigger signal, the refresh controller comprising:

an oscillator generating a first periodic clock signal;

a frequency division circuit coupled to receive the periodic clock signal, the frequency division circuit being operable to generate a second periodic clock signal having a frequency that is less than the frequency of the first periodic signal; and

a selector circuit coupled to receive the first periodic clock signal from the oscillator and the second periodic clock signal from the frequency division circuit, the first selector circuit being operable to apply the first periodic clock signal to an output terminal in the full density mode and to apply the second periodic clock signal to the output terminal in the reduced density mode, the refresh trigger signal being generated responsive to the periodic clock signal being coupled to the output terminal.

25. The dynamic random access memory of claim 24 wherein the selector circuit comprises:

a first pass gate coupled between an output of the oscillator and the output terminal;

a second pass gate coupled between an output of the frequency division circuit and the output terminal; and

a control circuit for enabling the first pass gate and disabling the second pass gate in the full density mode and for disabling the first pass gate and enabling the second pass gate in the reduced density mode.

26. The dynamic random access memory of claim 14 wherein the frequency divider circuit comprises a toggle flip-flop.

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27. A dynamic random access memory ("DRAM") comprising:

an array of memory cells arranged in rows and columns;

a column address latch structured to store a column address responsive to a column address strobe signal;

a column decoder coupled to the column address latch to receive the stored column address and enable respective sense amplifiers corresponding thereto;

a row address latch structured to store a row address responsive to a row address strobe signal;

a first row decoder coupled to the row address latch to receive the stored row address and activate respective word lines corresponding thereto, the first row decoder being enable responsive to a first enable signal;

a second row decoder coupled to the row address latch to receive the stored row address and activate respective word lines corresponding thereto, the row lines activated by the first row decoder being interleaved with the row lines activated by the second row decoder, the second row decoder being enabled responsive to a second enable signal;

a mode controller coupled to the row decoders, the mode controller being operable in a full density mode to generate the first enable signal responsive to a first state of a least significant bit of the row address and to generate the second enable signal responsive

to a second state of the least significant bit of the row address, the mode controller further being operable to generate the first and second enable signals in a reduced density mode regardless of the state of the least significant bit of the row address;

a data path coupled between the memory array and a data terminal; and

a refresh controller for refreshing at least some of the memory cells in the memory array responsive to a refresh trigger signal, the refresh controller comprising:

an oscillator generating a periodic clock signal;

a counter having a clock input terminal coupled to receive the clock signal, the counter having first and second stages the first of which increments at a faster rate than the second; and

a selector circuit coupled the first and second stages of the counter, the selector circuit being operable to couple the first stage of the counter to an output terminal in the full density mode and being operable to couple the second stage of the counter to the output terminal in the reduced density mode, the refresh trigger signal being generated responsive to the counter stage coupled to the output terminal by the selector circuit being incremented or decremented..

28. The dynamic random access memory of claim 27 wherein the selector circuit comprises:

a first pass gate coupled between the first stage of the counter and the output terminal;

a second pass gate coupled between the second stage of the counter and the output terminal; and

a control circuit for enabling the first pass gate and disabling the second pass gate in the full density mode and for disabling the first pass gate and enabling the second pass gate in the reduced density mode.

29. The dynamic random access memory of claim 27 wherein the second stage of the counter is two stages from the first stage of the counter so that the second stage is incremented at one-quarter the rate of the first stage.

30. A dynamic random access memory ("DRAM") comprising:

an array of memory cells arranged in rows and columns;

a circuit for remapping a specific row address bit to a specific column address bit, comprising:

a remapping latch coupled to receive the specific row address bit, the remapping latch being operable to store the specific row address bit responsive to a row address strobe signal and to then output the stored row address bit;

a column address latch coupled to receive a first set of column address bits and the specific column address bit, the column address latch being operable to store the first set of column address bits and the specific column address bit responsive to a column address strobe signal and to then output the stored column address bits, including the specific column address bit; and

a selector operable to select either the specific row address bit output from the remapping latch in a reduced density mode or the specific column address bit output from the column address latch in a full density mode, the selected address bit being combined with the column address bits in the first set to provide a composite column address;

a column decoder coupled to the selector to receive the composite column address and enable respective sense amplifiers corresponding thereto;

a row address latch structured to store a row address responsive to a row address strobe signal;

a first row decoder coupled to the row address latch to receive the stored row address and activate respective word lines corresponding thereto, the first row decoder being enable responsive to a first enable signal;

a second row decoder coupled to the row address latch to receive the stored row address and activate respective word lines corresponding thereto, the row lines activated by the first row decoder being interleaved with the row lines activated by the second row decoder, the second row decoder being enabled responsive to a second enable signal;

a mode controller coupled to the row decoders, the mode controller being operable in the full density mode to generate the first enable signal responsive to a first state of a least significant bit of the row address and to generate the second enable signal

responsive to a second state of the least significant bit of the row address, the mode controller further being operable to generate the first and second enable signals in the reduced density mode regardless of the state of the least significant bit of the row address; and

a data path coupled between the memory array and a data terminal.

31. The dynamic random access memory of claim 30 wherein the selector comprises:

a first pass gate coupled between an output of the first latch and an address output terminal;

a second pass gate coupled between an output of the second latch and the address output terminal; and

a control circuit for enabling the first pass gate and disabling the second pass gate or disabling the first pass gate and enabling the second pass gate.

32. A dynamic random access memory ("DRAM") comprising:

an array of memory cells arranged in rows and columns;

a column address latch structured to store a column address responsive to a column address strobe signal;

a column decoder coupled to the column address latch to receive the stored column address and enable respective sense amplifiers corresponding thereto;

a row address latch structured to store a row address responsive to a row address strobe signal;

a first row decoder coupled to the row address latch to receive the stored row address and activate respective word lines corresponding thereto, the first row decoder being enable responsive to a first enable signal;

a second row decoder coupled to the row address latch to receive the stored row address and activate respective word lines corresponding thereto, the row lines activated by the first row decoder being interleaved with the row lines activated by the second row decoder, the second row decoder being enabled responsive to a second enable signal;

a mode controller coupled to the row decoders, the mode controller being operable in the full density mode to generate the first enable signal responsive to a first state

of a least significant bit of the row address and to generate the second enable signal responsive to a second state of the least significant bit of the row address, the mode controller further being operable to generate the first and second enable signals in a reduced density mode regardless of the state of the least significant bit of the row address;

a data path coupled between the memory array and a data terminal; and

a refresh controller for refreshing at least some of the memory cells in the memory array responsive to a refresh trigger signal, the refresh controller comprising:

a toggle circuit receiving an auto refresh command and being structured to generate an enable signal responsive to only a portion of a plurality of auto-refresh commands;

a gate having a first input coupled to the toggle circuit and a second input receiving each of the plurality of auto-refresh commands, the gate being structured to generate a refresh signal responsive to each auto-refresh command when the gate is enabled by the enable signal from the toggle circuit.

33. A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a dynamic random access memory, comprising:

an array of memory cells arranged in rows and columns;

a column address latch structured to store a column address responsive to a column address strobe signal;

a column decoder coupled to the column address latch to receive the stored column address and enable respective sense amplifiers corresponding thereto;

a row address latch structured to store a row address responsive to a row address strobe signal;

a first row decoder coupled to the row address latch to receive the stored row address and activate respective word lines corresponding thereto, the first row decoder being enable responsive to a first enable signal;

a second row decoder coupled to the row address latch to receive the stored row address and activate respective word lines corresponding thereto, the row lines activated by the first row decoder being interleaved with the row lines activated by the second row decoder, the second row decoder being enabled responsive to a second enable signal;

a mode controller coupled to the row decoders, the mode controller being operable in a full density mode to generate the first enable signal responsive to a first state of a least significant bit of the row address and to generate the second enable signal responsive to a second state of the least significant bit of the row address, the mode controller further being operable to generate the first and second enable signals in a reduced density mode regardless of the state of the least significant bit of the row address;

a data path coupled between the memory array and a data terminal; and

a refresh controller for refreshing at least some of the memory cells in the memory array responsive to a refresh trigger signal, the refresh controller comprising:

an oscillator generating a first periodic clock signal;

a frequency division circuit coupled to receive the periodic clock signal, the frequency division circuit being operable to generate a second periodic clock signal having a frequency that is less than the frequency of the first periodic signal; and

a selector circuit coupled to receive the first periodic clock signal from the oscillator and the second periodic clock signal from the frequency division circuit, the first selector circuit being operable to apply the first periodic clock signal to an output terminal in the full density mode and to apply the second periodic clock signal to the output terminal in the reduced density mode, the refresh trigger signal being generated responsive to the periodic clock signal being coupled to the output terminal.

34. The computer system of claim 33 wherein the selector circuit comprises:

a first pass gate coupled between an output of the oscillator and the output terminal;

a second pass gate coupled between an output of the frequency division circuit and the output terminal; and

a control circuit for enabling the first pass gate and disabling the second pass gate in the full density mode and for disabling the first pass gate and enabling the second pass gate in the reduced density mode.

35. The computer system of claim 33 wherein the frequency divider circuit comprises a toggle flip-flop.

36. A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a dynamic random access memory, comprising:

an array of memory cells arranged in rows and columns;

a column address latch structured to store a column address responsive to a column address strobe signal;

a column decoder coupled to the column address latch to receive the stored column address and enable respective sense amplifiers corresponding thereto;

a row address latch structured to store a row address responsive to a row address strobe signal;

a first row decoder coupled to the row address latch to receive the stored row address and activate respective word lines corresponding thereto, the first row decoder being enable responsive to a first enable signal;

a second row decoder coupled to the row address latch to receive the stored row address and activate respective word lines corresponding thereto, the row lines activated by the first row decoder being interleaved with the row lines activated by the second row decoder, the second row decoder being enabled responsive to a second enable signal;

a mode controller coupled to the row decoders, the mode controller being operable in the full density mode to generate the first enable signal responsive to a first state of a least significant bit of the row address and to generate the second enable signal responsive to a second state of the least significant bit of the row address, the mode controller further being operable to generate the first and second enable signals in a reduced density mode regardless of the state of the least significant bit of the row address;

a data path coupled between the memory array and a data terminal; and

a refresh controller for refreshing at least some of the memory cells in the memory array responsive to a refresh trigger signal, the refresh controller comprising:

an oscillator generating a periodic clock signal;

a counter having a clock input terminal coupled to receive the clock signal, the counter having first and second stages the first of which increments at a faster rate than the second; and

a selector circuit coupled the first and second stages of the counter, the selector circuit being operable to couple the first stage of the counter to an output terminal in the full density mode and being operable to couple the second stage of the counter to the output terminal in the reduced density mode, the refresh trigger signal being generated responsive to the counter stage coupled to the output terminal by the selector circuit being incremented or decremented.

37. The computer system of claim 36 wherein the selector circuit comprises:

a first pass gate coupled between the first stage of the counter and the output terminal;

a second pass gate coupled between the second stage of the counter and the output terminal; and

a control circuit for enabling the first pass gate and disabling the second pass gate in the full density mode and for disabling the first pass gate and enabling the second pass gate in the reduced density mode.

38. The computer system of claim 36 wherein the second stage of the counter is two stages from the first stage of the counter so that the second stage is incremented at one-quarter the rate of the first stage.

39. A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a dynamic random access memory, comprising:

an array of memory cells arranged in rows and columns;

a circuit for remapping a specific row address bit to a specific column address bit, comprising:

a remapping latch coupled to receive the specific row address bit, the remapping latch being operable to store the specific row address bit responsive to a row address strobe signal and to then output the stored row address bit;

a column address latch coupled to receive a first set of column address bits and the specific column address bit, the column address latch being operable to store the first set of column address bits and the specific column address bit responsive to a column address strobe signal and to then output the stored column address bits, including the specific column address bit; and

a selector operable to select either the specific row address bit output from the remapping latch in a reduced density mode or the specific column address bit output from the column address latch in a full density mode, the selected address bit being combined with the column address bits in the first set to provide a composite column address;

a column decoder coupled to the selector to receive the composite column address and enable respective sense amplifiers corresponding thereto;

a row address latch structured to store a row address responsive to a row address strobe signal;

a first row decoder coupled to the row address latch to receive the stored row address and activate respective word lines corresponding thereto, the first row decoder being enable responsive to a first enable signal;

a second row decoder coupled to the row address latch to receive the stored row address and activate respective word lines corresponding thereto, the row lines activated by the first row decoder being interleaved with the row lines activated by the second row decoder, the second row decoder being enabled responsive to a second enable signal;

a mode controller coupled to the row decoders, the mode controller being operable in the full density mode to generate the first enable signal responsive to a first state of a least significant bit of the row address and to generate the second enable signal responsive to a second state of the least significant bit of the row address, the mode controller further being operable to generate the first and second enable signals in the reduced density mode regardless of the state of the least significant bit of the row address; and

a data path coupled between the memory array and a data terminal.

40. The computer system of claim 39 wherein the selector comprises:

a first pass gate coupled between an output of the first latch and an address output terminal;

a second pass gate coupled between an output of the second latch and the address output terminal; and

a control circuit for enabling the first pass gate and disabling the second pass gate or disabling the first pass gate and enabling the second pass gate.

41. A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a dynamic random access memory, comprising:

an array of memory cells arranged in rows and columns;

a column address latch structured to store a column address responsive to a column address strobe signal;

a column decoder coupled to the column address latch to receive the stored column address and enable respective sense amplifiers corresponding thereto;

a row address latch structured to store a row address responsive to a row address strobe signal;

a first row decoder coupled to the row address latch to receive the stored row address and activate respective word lines corresponding thereto, the first row decoder being enable responsive to a first enable signal;

a second row decoder coupled to the row address latch to receive the stored row address and activate respective word lines corresponding thereto, the row lines activated by the first row decoder being interleaved with the row lines activated by the second row decoder, the second row decoder being enabled responsive to a second enable signal;

a mode controller coupled to the row decoders, the mode controller being operable in the full density mode to generate the first enable signal responsive to a first state of a least significant bit of the row address and to generate the second enable signal responsive to a second state of the least significant bit of the row address, the mode controller further being operable to generate the first and second enable signals in a reduced density mode regardless of the state of the least significant bit of the row address;

a data path coupled between the memory array and a data terminal; and

a refresh controller for refreshing at least some of the memory cells in the memory array responsive to a refresh trigger signal, the refresh controller comprising:

a toggle circuit receiving an auto refresh command and being structured to generate an enable signal responsive to only a portion of a plurality of auto-refresh commands;

a gate having a first input coupled to the toggle circuit and a second input receiving each of the plurality of auto-refresh commands, the gate being structured to generate a refresh signal responsive to each auto-refresh command when the gate is enabled by the enable signal from the toggle circuit.

42. A method of refreshing a dynamic random access memory ("DRAM") having a full density operating mode and a reduced density operating mode, the method comprising:

determining the operating mode of the DRAM;

if the DRAM is determined to be operating in the full density mode, refreshing the DRAM at a first rate; and

if the DRAM is determined to be operating in the reduced density mode, refreshing the DRAM at a second rate, the second rate being slower than the first rate.

43. The method of claim 42 wherein the second rate is 8 times slower than the first rate.

44. A method of addressing a dynamic random access memory ("DRAM") having a full density operating mode and a reduced density operating mode, the method comprising:

determining the operating mode of the DRAM;

storing a specific row address bit responsive to a row address strobe signal;

storing a first set of column address bits and a specific column address bit responsive to a column address strobe signal; and

in the full density operating mode, selecting the first set of column address bits and the specific column address bit that were stored responsive to the column address strobe signal;

in the reduced density operating mode, selecting the first set of column address bits that were stored responsive to the column address strobe signal and the specific row address bit that was stored responsive to the row address strobe signal; and

addressing a column of the the DRAM using the selected address bits.

45. The method of claim 44, further comprising addressing a row of the DRAM, the method comprising:

storing a second set of row address bits along with the specific row address bit responsive to the row address strobe signal; and

addressing a row of the DRAM using the stored second set of row address bits.

46. A method of refreshing a dynamic random access memory ("DRAM") having a full density operating mode and a reduced density operating mode, the method comprising:

applying a plurality of auto-refresh commands to the DRAM;

determining the operating mode of the DRAM;

if the DRAM is determined to be operating in the full density mode, refreshing the DRAM responsive to each of the plurality of auto-refresh commands; and

if the DRAM is determined to be operating in the reduced density mode, refreshing the DRAM responsive to less than each of the plurality of auto-refresh commands.

47. The method of claim 46, wherein the act of refreshing the DRAM responsive to less than each of the plurality of auto-refresh commands comprises refreshing the DRAM responsive to half of the plurality of auto-refresh commands.